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ENABLING DESIGN

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Advanced VHDL Testbenches and Verification (5-day course)

A thorough introduction and overview of advanced VHDL verification techniques and methodology, using OSVVM. 50/50 labs and lecture

OSVVM

Overview

Learn the latest VHDL Verification techniques and methodologies for FPGAs and ASICs, including the Open Source VHDL Verification Methodology (OSVVM).

You will gain the knowledge needed to improve your verification productivity and create a VHDL testbench environment that is competitive with other verification languages, such as SystemVerilog (UVM).

Unlike UVM, our methodology works with any simulator that supports VHDL-2008, removing the requirement to learn a new language or invest in new and costly tools.

Who should attend?

Suitable for digital (FPGA/ASIC/PLD) designers with a requirement to improve verification efficiency and effectiveness.

Prerequisites

Delegates should have a good working knowledge of digital circuits and prior experience of VHDL through work or a previous training course.

Content and Structure

You will learn how to create structured transaction-based testbenches using either procedures or models (aka: verification IP or transaction level models). Both methods facilitate creation of simple, powerful, and readable tests.

You will also learn about subprogram usage, libraries, file reading and writing, error reporting (Alerts and Affirmations), message handling (logs), abstractions for interface connectivity (records and resolution functions), model synchronisation methods (barrier synchronisation and others), verification data structures (scoreboards and FIFOs), directed, algorithmic, constrained random, coverage driven random test generation, self-checking (result, timing, protocol checking and error injection), functional coverage, representation of analogue values and periodic waveforms (such as triangle or sine waves), and test planning.

The course then progresses onto advanced topics including, modeling multi-threaded models (such as AXI4-Lite), advanced functional coverage, advanced randomisation, creating data structures using protected types and access types, timing and execution, configurations and modeling RAM.

This training is modular and can be split into two separate courses. The first three days of this training can be attended standalone, as our Essential VHDL Verification course. Once delegates have attended Essential VHDL Verification, they can then attend a further 2-day Expert VHDL Verification course. Together, these two courses are equivalent to Advanced VHDL Testbenches and Verification.

Day 1, Module CT1
- Overview
- Basic testbenches
- Transactions and subprograms
- Modelling for verification
- OSVVM error & message handling

- Labs:
  -Testing UartTx using subprograms

Day 2, Module CT2
- Lab review: testing w/ subprograms
- Transaction-based models
- Elements of a transaction-based model
- Writing tests & self-checking
- Labs:
  -UartTx model (verification IP),
  -Injecting errors in the UART
  -Using OSVVM's Scoreboard

Day 3, Module CT3
- Lab review: UartTx BFM
- Constrained random testing
- Functional coverage
- Planning and reuse
- OSVVM library
- Lab review: scoreboard, random
- Functional coverage
- Labs:
  -Adding functional coverage
  -Adding constrained and intelligent random
  -reuse & subblock testing

Day 4, Module AT1
- Advanced modelling w/ AXI-Lite master
- Simulation management and configurations
- Data structures and protected types
- Advanced coverage techniques
- Labs:
  -AXI-Stream

Day 5, Module AT2
- Execution and timing
- Advanced randomisation
- Modelling RAM
- Interrupt handling
- Validating self-checking models
- Labs:
  -AXI-Stream

Approach and Labs

This hands-on, how-to course is taught by an experienced verification engineer with specialist VHDL knowledge and expertise. We believe that student and instructor interaction is key to a successful learning environment, therefore places on public courses are limited.

The training is split roughly 50/50 lecture and labs, so plenty of opportunity to reinforce the theory. Each delegate will be provided with access to a laptop, Aldec Riviera-PRO and all the necessary resources required for successful completion.

The trainer

Developed and delivered by Jim Lewis, chair of the IEEE VHDL standards working group and chief architect of OSVVM, this training gives you the deep insight into the methodology that is only available from its developers.