FIRSTEDA
ENABLING DESIGN

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Intermediate VHDL
(Remote online course - 5 days)

Designed to bridge the gap between possessing a basic working knowledge of VHDL and our Advanced VHDL Testbenches & Verification course

Overview

Ready for the next step?
For those already familiar with VHDL, either through introductory training or self-taught, this course will broaden knowledge and enforce competency through application.

Delivered remotely online, this live and interactive instructor-led training is specifically constructed to bridge the gap between basic working knowledge of VHDL and our Advanced VHDL Testbenches & Verification course.

As part of our well regarded VHDL training series, our courses are all delivered by time-served engineers in the field of language-based design & verification. Our methodology experts are able to provide insights that go beyond theory, and this ensures practical benefit is gained immediately.

Objectives

- To provide practical experience in writing, testing and synthesing VHDL code as well as how to implement it on an FPGA
- To enhance your current understanding of VHDL through problematic hardware coding issues
- To introduce you to transaction-based testbenches
- To introduce FSM coding techniques
- To provide VHDL hardware experience with an FPGA lab board

Prerequisites

Delegates should be familiar with digital design and have a basic understanding of VHDL. Although not essential, an understanding of other HDL or programming languages is an advantage. As this course is delivered live online, each delegate will require access to a personal computer with a reliable and stable internet connection.

Content and structure

Delivered over 5 days, with 2.5 hours scheduled daily for live and interactive lecture sessions, led by our expert trainer. This course is designed to build upon existing VHDL knowledge acquired through hands-on experience, or through introductory VHDL training such as our VHDL for FPGA Designers course.

The training covers both syntax and coding style guidelines in depth, followed by practical exercises designed specifically to reinforce the lecture material. Design projects utilise all techniques learned in the lectures and demonstrate how VHDL is used in a project environment.

Day 1
- **Lab review**
- Designing with VHDL
- Data Types
- **Case Study:** SwitchDebounce State machine

Day 2
- **Lab review**
- RTL Essentials
- Data Objects

Day 3
- **Lab review**
- Testbench Essentials
- Subprograms

Day 4
- **Lab review**
- Testbenches & Timing
- VHDL IO

Day 5
- RTL Code
- Numeric Types
- Design Organisation
- **Lab review**

Course labs

Practical labs account for 50% of the course material and range from simple simulation and synthesis coding problems through to small design projects. Utilising all the techniques imparted in the lectures, the labs provide invaluable hands-on experience of writing RTL code, developing VHDL testbenches, running simulation and programming an FPGA development board. For the lab excersises, delegates utilise either Aldec Active-HDL or Riviera-PRO. Both of which are intuitive class-leading FPGA design and simulation environments.

Delegate takeaways

Delegates are provided in advance with a high quality lecture book and detailed lab book, supporting all of the material covered during the course. An FPGA development board is used during the lab exercises and can be kept after the course to further expand VHDL knowledge through the takeway labs.