FIRSTEDA
ENABLING DESIGN

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VHDL for FPGA Designers (2-day course)

Our introductory VHDL language training, for those with no prior experience of writing VHDL - 50/50 labs and lecture

Introduction

What is VHDL?
VHDL is not a software programming language, it is an HDL - a Hardware Description Language, used to describe electronics hardware for implementation in FPGA or ASIC digital devices.

Overview

Our two (2) day instructor led VHDL language and application training provides a thorough background in the use and application of synthesisable VHDL in digital hardware design. The training is structured around a set of basic component building blocks and uses these devices to demonstrate the application of the VHDL language.

This is the first part of our VHDL training series, covering basic concepts and syntax relating to the circuit structures covered, and gives the FPGA designer sufficient knowledge to start writing synthesisable VHDL upon successful completion of the course. We also provide additional VHDL training classes which cover the more advanced language constructs and methodologies.

Objectives

- To provide a complete understanding of the basic concepts in VHDL
- To introduce you to the syntax and language building blocks based on a number of common circuit elements
- To give you practical experience of writing and verifying simple VHDL designs

Duration

Our standard course is based around a two-day agenda. As the material is highly modular, we can also offer customised versions of this course, on-site or at a location of your choice.

Requirements

Delegates should have a basic knowledge of using a PC running the Microsoft® Windows® operating system. The course assumes no prior knowledge of VHDL but experience of other software languages is useful (but not essential).

Description

This course covers the fundamental principles of the VHDL language and the constructs most commonly used in synthesisable Register Transfer Level (RTL) design.

Agenda

- The History of VHDL
- VHDL as a Programming Language
- VHDL in the Design Process
- First VHDL Design - MUX2
- More Combinational Designs
- Processes
- More Sequential Statements
- Concurrent Statements
- Hierarchy
- Simple Testbenches
- Packages
- Finite State Machines

Course Labs

The individual labs have been designed to logically develop over the course of the training, building on code developed in each successive lab to create an overall design project.

The labs utilise Aldec Active-HDL, the intuitive class-leading FPGA design and simulation environment, to follow the basic steps required to create and simulate a small design.

Delegate Takeaways

As one of the deliverables, each delegate is given a high quality colour printed training notebook containing all the material covered during the course. This notebook will prove an invaluable resource as you start your HDL design journey. Each delegate will also be provided with a high quality colour printed A5 lab workbook, the files they created during the training, the solutions for the lab exercises as well as a useful library of basic VHDL components to enable delegates to expand their knowledge once they have left the classroom.