FIRSTEDA
ENABLING DESIGN

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FPGA Design & Verification in Aldec Active-HDL (2-day course)

For all Active-HDL users; This course covers everything you need to know for your day-to-day FPGA design, verification, analysis and documentation tasks

Introduction

This two (2) day instructor led training course will give the delegate a general introduction to Aldec's class-leading Active-HDL FPGA design creation and simulation platform. Once completed, the engineer will be able to create and manage new FPGA designs, run simulations, analyse results and debug their work.

Overview

This application training provides a basic understanding of all the design entry methods within Active-HDL (HDL code , Block Diagram & Finite State Machine). The flow continues, using the design files created, to progress through the simulation and debug environment. This enables the delegate to get a full understanding of how to use Active-HDL effectively for the day-to-day FPGA design, verification, analysis and documentation tasks.

Testbench creation is covered and we look at both functional and toggle code coverage as well as HDL Design Rule Checking using the ALINT tool. Creating effective documentaion is one of the stand-out features of Active-HDL and this is covered thoroughly in the wrap-up.

Objectives

- To provide a complete understanding of the basic concepts of Active-HDL
- To introduce you to the tools and methodologies within Active-HDL and to give you practical experience of applying them on simple HDL designs

Duration

Our standard course is based around a two-day agenda. As the material is highly modular, we can also offer customised versions of this course, on-site or at a location of your choice.

Requirements

Delegates should have a basic knowledge of using a PC running the Microsoft® Windows® operating system. The course assumes no prior knowledge of Aldec Active-HDL but experience of VHDL or other FPGA design software is useful (but not essential).

Description

This course covers the fundamental principles of the VHDL language and the constructs most commonly used in synthesisable Register Transfer Level (RTL) design.

Agenda

- Project Management
- Design Entry - HDL Code
- Design Entry - BDE (Block Diagram)
- Design Entry - FSM (Finite State Machine)
- Design Entry - Advanced BDE
- Design Entry - Advanced FSM
- Running Simulation
- Waveform Display
- Design Verification
- Creating Testbenches
- Code & Toggle Coverage
- ALINT-PRO - HDL Design Rule Checking
- Documentation Features

Course Labs

The course labs will familiarise you with Active-HDL, building on the knowledge learned during the lecture sessions. The lab workbook provides step-by-step instructions to guide you through every stage of using the tools; design entry, simulation, analysis and documentation.

Delegate Takeaways

As one of the deliverables, each delegate is given a high quality colour printed training notebook containing all the material covered during the course. This notebook will prove an invaluable resource as you start your HDL design journey. Each delegate will also be provided with a high quality colour printed A5 lab workbook, the files they created during the training, the solutions for the lab exercises as well as a useful library of basic VHDL components to enable delegates to expand their knowledge once they have left the classroom.