FIRSTEDA
ENABLING DESIGN

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Essential VHDL Verification (3-day course)

A thorough introduction and overview of essential VHDL verification techniques and methodology, using OSVVM - 50/50 labs and lecture

Overview

Learn the latest VHDL verification techniques and methodologies for FPGAs and ASICs, including the Open Source VHDL Verification Methodology (OSVVM).

You will gain the knowledge needed to improve your verification productivity and create a VHDL testbench environment that is competitive with other verification languages, such as SystemVerilog (UVM).

Unlike UVM, our methodology works with any simulator that supports VHDL-2008, removing the requirement to learn a new language or invest in new and costly tools.

Who should attend?

Suitable for digital (FPGA/ASIC/PLD) designers with a requirement to improve verification efficiency and effectiveness.

Prerequisites

Delegates should have a good working knowledge of digital circuits and prior experience of VHDL through work or a previous training course.

Content & Structure

You will learn how to create structured transaction-based testbenches using either procedures or models (aka verification IP or transaction-level models). Both methods facilitate creation of simple, powerful, and readable tests.

You will also learn about subprogram usage, libraries, file reading and writing, error reporting (Alerts & Affirmations), message handling (logs), abstractions for interface connectivity (records & resolution functions), model synchronisation methods (barrier synchronisation & others), verification data structures (scoreboards & FIFOs), directed, algorithmic, constrained random, coverage-driven random test generation, self-checking (result, timing, protocol checking & error injection), functional coverage, representation of analogue values and periodic waveforms (such as triangle or sine waves), and test planning.

Essential VHDL Verification is effective as a stand-alone 3-day course, but also forms the first 3 days of our comprehensive 5-day Advanced VHDL Testbenches and Verification training.

Day 1, Module CT1

- Overview
- Basic testbenches
- Transactions & subprograms
- Modelling for verification
- OSVVM error & message handling
- Labs:
  -Testing UartTx using subprograms

Day 2, Module CT2

- Lab review: testing w/ subprograms
- Transaction-based models
- Elements of a transaction-based model
- Writing tests & self-checking
- Labs:
  -UartTx model (verification IP)
  -Injecting rrrors in the UART
  -Using OSVVM's scoreboard

Day 3, Module CT3

- Lab review: UartTx BFM
- Constrained random testing
- Functional coverage
- Planning & reuse
- OSVVM library
- Lab review: scoreboard, random
- Functional coverage
- Labs:
  -Adding functional coverage
  -Adding constrained and intelligent random
  -Reuse & subblock testing

Approach & Labs

This hands-on, how-to course is taught by an experienced verification engineer with specialist VHDL knowledge and expertise. We believe that student and instructor interaction is key to a successful learning environment, therefore places on public courses are limited.
The training is split roughly 50/50 lecture and labs, so plenty of opportunity to reinforce the theory. Each delegate will be provided with access to a laptop, Aldec Riviera-PRO and all the necessary resources required for successful completion.

The Trainer

Developed and delivered by Jim Lewis, chair of the IEEE VHDL standards working group and chief architect of OSVVM, this training gives you the deep insight into the methodology that is only available from its developers.