HES-DVM™ | HW/SW Validation Platform

Hybrid Verification Platform

HES-DVM™ is a hybrid verification and validation platform for hardware and software developers of SoC and ASIC designs. Utilizing the industry-proven co-emulation standards like SCE-MI or TLM and the newest Xilinx® FPGA technology, HES-DVM provides a high-speed emulation solution for pre-silicon test and debug with hardware speeds, real-time data interfaces, and an automated design setup environment. Partnered with HDL simulators, virtual platforms, hardware and software debuggers, and a library of synthesizable transactors and speed adapters, design teams are able to reduce the verification cycle and risks of silicon re-spins.

Top Features

- **Scalable FPGA hardware platform utilizing the newest and largest Xilinx devices**

- **Versatile applications: Simulation Acceleration, Hybrid Co-Emulation, ICE, Physical Prototyping**

- **Transaction level standards support facilitating design of reusable transactors (SCE-MI, TLM)**

- **Extensive debugging with full visibility into FPGA and memory viewer**

- **Automated design setup with multi-FPGA partitioning and interconnections**

- **Patented clock conversion algorithm for reliable FPGA implementations and board-level timing closure**

- **Linux and Windows® environment support**

Acceleration, Emulation, and Prototyping

HES-DVM combines high end FPGA prototyping boards utilizing newest and largest Xilinx FPGA chips with multiple modes of operation including Simulation Acceleration, Hybrid Co-Emulation, In-Circuit-Emulation and Physical Prototyping. High speed backplane solution makes the hardware scalable and appropriate for block level or chip level verification of SoC and ASIC designs. The functionality of hardware can be easily extended with reach choice of Daughter Cards making the HES-DVM platform the most versatile and cost effective on the market.

Software Development with Complete SoC and Hardware Prototype

Software developers today need an early access to the SoC hardware prototype to develop and debug applications that should be run on the latest OS or RTOS. Combining QEMU or Virtual Platform with HES-DVM, developers are able to connect virtual processor models with custom hardware RTL blocks using high speed bus transactors like AMBA AXI or AHB. Partnering such a hybrid hardware model with fully integrated array of debugging tools that enable full visibility, developers are able to load applications to program memory, decreasing overall system boot-time or check state of essential system registers directly in FPGA to validate required functionality or trace hardware related malfunctions.

HES™ BUNDLE PACKAGES

Elite

DVM-Elite Base Package

- Emulation Mode
- In Circuit Emulation
- Multi-engine emulation
- Simulation Acceleration - Transaction Level
- Simulation Acceleration Mode – Signal Level
- Hybrid Co-emulation with Virtual Platforms
- Prototyping Mode
- Accellera SCE-MI Interface
- Aldec simulators: Active-HDL, Riviera-PRO
- UVM, System Verilog, Verilog, VHDL, SystemC, TLM support
- Automated Design Partitioning
- Automated Interconnections
- Gated Clock Conversion
- Memory Model Mapping
- Static Debugging Probes
- Dynamic Debugging Probes
- Memory Viewer
- Hardware Debugger Tool
- HES Debug API
- Linux and Windows

Optional

- Custom Board Support
- Other Vendor Simulators
- ARM Fast Models Co-emulation
- QEMU Co-emulation
- OVP Co-emulation
- Transactors & Speed Adapters

Emulation

DVM-EMU Base Package

- Emulation Mode
- In Circuit Emulation
- Multi-engine emulation
- Simulation Acceleration - Transaction Level
- Hybrid Co-emulation with Virtual Platforms
- Accellera SCE-MI Interface
- Aldec simulators: Active-HDL, Riviera-PRO
- UVM, System Verilog, Verilog, VHDL, SystemC, TLM support
- Automated Design Partitioning
- Automated Interconnections
- Gated Clock Conversion
- Memory Model Mapping
- Static Debugging Probes
- Dynamic Debugging Probes
- Memory Viewer
- Hardware Debugger Tool
- HES Debug API
- Linux and Windows

Optional

- Other Vendor Simulators
- ARM Fast Models Co-emulation
- QEMU Co-emulation
- OVP Co-emulation
- Transactors & Speed Adapters

Acceleration

DVM-XL Base Package

- Simulation Acceleration Mode – Signal Level
- Aldec simulators: Active-HDL, Riviera-PRO
- System Verilog, Verilog, VHDL, SystemC support
- Daughter Card Connection
- Automated Design Partitioning
- Automated Interconnections
- Mirror-Box & Black-Box Functionality
- Gated Clock Conversion
- Memory Model Mapping
- Static Debugging Probes
- Dynamic Debugging Probes
- Memory Viewer
- Hardware Debugger Tool
- HES Debug API
- Linux and Windows

Optional

- Other Vendor Simulators

Prototyping

DVM-PROTO Base Package

- Prototyping Mode
- Daughter Card Connection
- Automated Design Partitioning
- Automated Interconnections
- Gated Clock Conversion

Optional Proto Extensions

- Multiple-FPGA Board Support

Scalable HES FPGA Boards with Xilinx Virtex UltraScale, Virtex-7 and Backplane

HES-7, HES-US or Custom FPGA Prototyping Boards

Optional SCE-MI Transactors and Speed Adapters

Bus Protocol Transactor Models Available
AHB (AMBA 2.0) OCP, Wishbone, AXI4 (AMBA 4.0), AXI3 (AMBA 3.0), AXI4-Lite (AMBA 4.0)

Peripheral Transactor Models Available
UART, I2C, I2S, JTAG, SPI, SDIO,USB 2.0

Networking Transactor Models Available
10/100/1000 Gigabit Ethernet

Video Transactor Models Available
CCIR656 Image Sensor, HDMI 1.2a Source and Sink 1080p60, HDMI 1.3a Source and Sink 2560x1600p60

Serial Link Transactor Models Available
PCIe 2.0/1.1 endpoint, PCIe 2.0/1.1 rootport

MEMS Transactor Models Available
Accelerometer (G-Sensor), Gyrometer (Gyros)

Speed Adapter Models Available
SPI4.2, CSIX, PCIe Gen2, 1-wire, JTAG

Hardware Boards

HES-7 (Virtex-7 based)
HES7XV1380BP (~8M ASIC Gates)
HES7XV4000BP (~24M ASIC Gates)
HES7XV12000BP (~72M ASIC Gates)
Scalable with backplane up to ~288M ASIC Gates
HES-US (Virtex UltraScale based)
HES-US-440 (~26M ASIC Gates)
HES-US-1320 (~79M ASIC Gates)
HES-US-2640 (~158M ASIC Gates)
Scalable with backplane up to ~633M ASIC Gates
Daughter Cards & Interfaces
Xilinx Zynq with ARM Cortex
PCIe, USB, SATA
Gigabit Ethernet, QSFP+, Wireless for IoT
HDMI, Display Port, Multimedia & Vision

https://www.aldec.com/en/products/prototyping

STANDARDS

accellera SYSTEMS INITIATIVE | IEEE | SYSTEMC | SystemVerilog

PARTNERS

ARM | ANDES TECHNOLOGY | NORTHWEST LOGIC | HELION | CREONIC | XILINX

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