FIRSTEDA
ENABLING DESIGN
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concept engineering

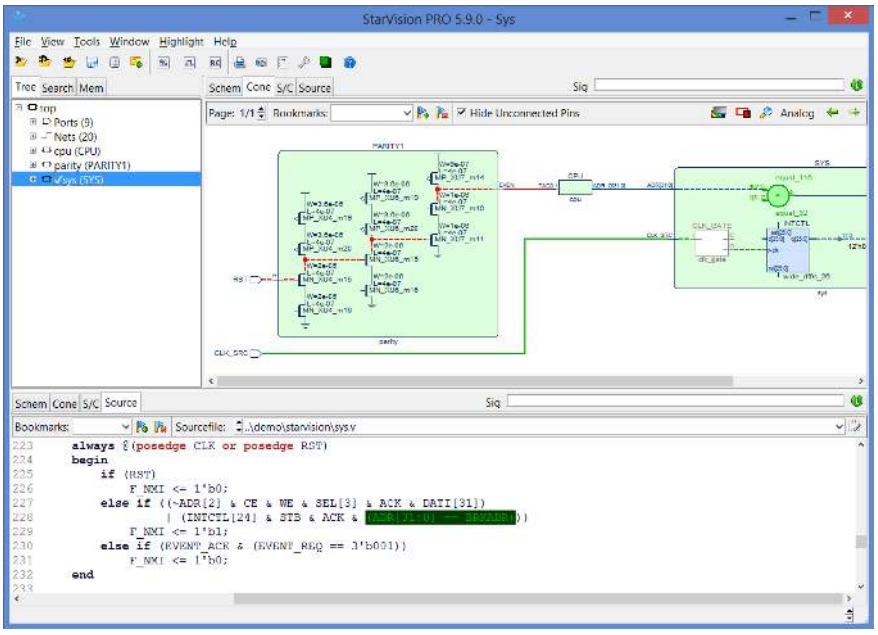
STARVISION® PRO

StarVision™ PRO: A Customizable Mixed-Signal Debugger

StarVision PRO provides engineers with the ability to quickly and easily understand and debug mixed-mode designs and to integrate IP building blocks into their complex SoCs and ICs.

All-in-One – Due to the increasing use of building blocks in SoC design, engineers need to work at different design levels (RTL, gate, transistor, analog, parasitic) as well as with different design languages and netlist formats. To support this challenge, Concept Engineering developed StarVision PRO, an integrated debugging cockpit for mixed-signal and digital design that makes analysis and debugging of complex SoC and IC designs easy and more transparent.

Easy Design Exploration – The interactive design navigation window shows schematic fragments of just the critical portion of the design while, at the same time, providing links to the original source code fragments (RTL, Netlist, SPICE) and to simulation results.



- SystemVerilog, VHDL, SPICE, HSPICE®, ELDO, Spectre®, DSPF, SPEF
- RTL viewer, Netlist viewer and SPICE viewer in one tool
- Mixed-Signal Debugger – Makes IP-based design more transparent
- 32/64-bit database handles today's largest SoCs and ASICs
- Integrated Waveform Viewer with source code link and schematic link
- Interactive schematic window displays selected fragments and critical paths
- Automatic Logic Recognition – Reads SPICE and shows logic functions
- Tcl based API for user-defined electrical rule checks and customization

Clock Tree Extraction – Clock signals are often a source of problems in complex SoC design. StarVision PRO automatically extracts and analyzes clock trees and gives an immediate view of clock trees and clock domains.

Waveform Viewer and Signal Tracing – StarVision PRO comes with a fully integrated waveform browser and with support for interactive signal tracing in the source code, schematic view and waveform window. StarVision PRO compiles VCD simulation data into its own high-speed format for accelerated waveform browsing and signal tracing.

Path Extraction – The customizable path extraction engine can automatically identify and extract critical paths in a design. These can be explored and cross-probed in different views to reduce both the complexity and time of the debug cycle.

Automatic Logic Recognition – The built-in automatic logic recognition engine creates digital logic schematics from pure SPICE-level netlists for easy design exploration.

Customization – Users can write API code to analyze the design and generate user-specific design reports and design rule checks.

Improved Productivity – Being able to analyze RTL-level, gate-level and transistor-level at the same time in just one debug cockpit increases design and verification engineers productivity, reducing product development time and debug cycle time.

At a Glance

FEATURE	BENEFITS
Ultra fast HDL reader and graphics on the fly	Graphical representations make it easier to understand, debug, change and optimize Verilog, VHDL and SystemVerilog code
Schematics from SPICE netlists	Schematics provide easier and faster debugging for complex circuits. Supported dialects include SPICE, HSPICE®, Calibre®, CDL, Eldo and Spectre®.
32/64-bit database	Higher performance and increased capacity, for very large designs
Powerful GUI	Multiple views, including tree, schematic, waveform and source file plus drag and drop between different views for increased circuit understanding
Cone Window	Incremental schematic navigation for easy design exploration
Tcl UserWare API	Allows interfacing with tool flow and definition of electrical rule checks
Circuit fragment save	Circuit netlists can be saved as SPICE files or Verilog files for future reuse as IP, or for partial simulation
Automatic clock tree and clock domain extraction and visualization	Faster detection and resolution of clock domain problems
Full support for mixed language and mixed-signal designs	Designers can easily debug today's most complex heterogeneous designs (SystemVerilog, Verilog, VHDL, SPICE, HSPICE®, Spectre®,EDIF …)
Parasitic analysis option	Allows visualization and analysis of parasitic networks (SPEF, DSPF) and provides capabilities to create SPICE netlists for circuit fragments

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