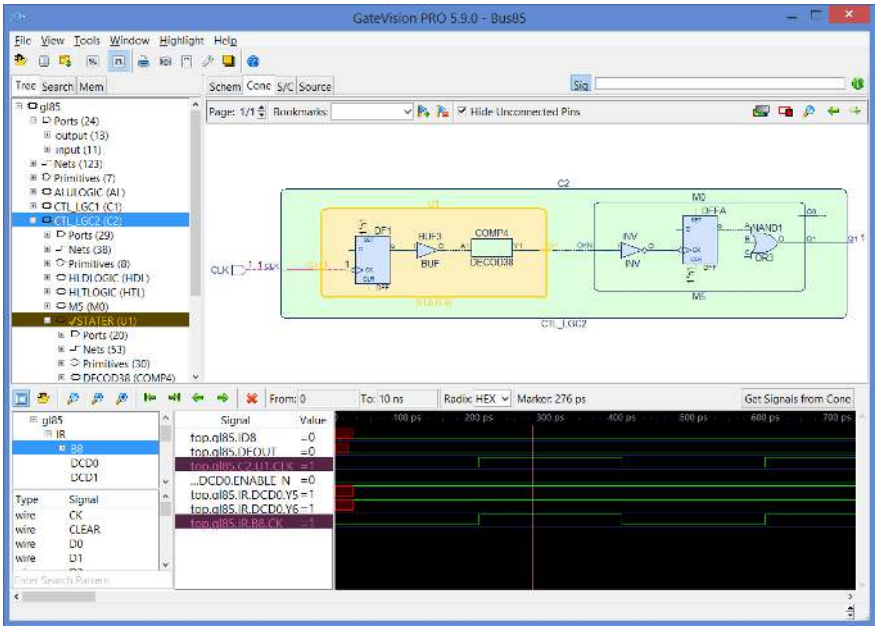
FIRSTEDA
ENABLING DESIGN
FirstEDA Limited, Eastlands II, London Rd, Basingstoke, RG21 4AW, UK
t: +44 (1295) 201250 / e: info@firsteda.com / w: www.firsteda.com

concept engineering

GATEVISION® PRO

GateVision® PRO: New Power for Gate-Level Debugging and Netlist Viewing

GateVision PRO is the third generation of graphical netlist analyzers from Concept Engineering. GateVision PRO provides the designer of even the largest SoCs with intuitive design navigation, schematic viewing, logic cone extraction and waveform viewing for debug support, fast design exploration, and design documentation.



- Extreme performance netlist viewer for Verilog, EDIF, and LEF/DEF
- Tcl based UserWare API – for advanced customization and ERC
- 32/64 bit database handles today's largest SoCs, ASICs and FPGAs
- Integrated Waveform Browser (accelerated VCD viewer)
- Customizable path extraction engine finds critical paths
- Cone view displays schematic fragments of critical areas
- Intuitive GUI for ease of use
- Flexible netlist export features

Ultra Fast Netlist Viewing – Reading Verilog, EDIF, and LEF/DEF netlists, GateVision PRO fits seamlessly into any design environment. Schematics are generated on the fly and the intuitive GUI lets the designer incrementally and easily navigate through the largest netlist files.

Clock Tree Extraction – Clock signals are often a source of problems when integrating IP building blocks from different sources; GateVision PRO automatically extracts clock trees and gives an immediate view of the clock network and clock domains.

Verilog Netlist Export – Critical path fragments can be isolated and exported as Verilog netlist files for fast and precise critical path simulation.

Waveform Viewer and Signal Tracing – GateVision PRO comes with a fully integrated waveform viewer and with support for interactive signal tracing in the source code, schematic view and waveform window. GateVision PRO compiles VCD simulation data into its own high-speed format for accelerated waveform browsing and signal tracing.

Logic Cone – The GateVision PRO logic cone provides interactive navigation within a schematic fragment, that portion of the circuit that is most relevant. Such fragments can be extended and reduced for signal path tracing through the complete design hierarchy.

Path Extraction and Verilog Simulation – The customizable path extraction engine automatically extracts critical paths in a design. These can be explored and cross-probed in different views to reduce both the complexity and time of the debug cycle. Path fragments can be exported as Verilog netlists for critical path Verilog simulation.

Customization – Users can write API code (Tcl programming language) to analyze the design data and to generate user-specific design reports, electrical design rule checks (ERC), and to interface with other EDA tools.

Debugging Views – Built into GateVision Pro are a variety of view options, including schematic view, schematic fraction view, source code view, hierarchy tree view, waveform view, clock domain view, and object search view. Through these, and through cross-probing between views, it is easy to gain a deeper understanding of the device being debugged and to find logic or timing problems.

At a Glance

FEATURE	BENEFITS
Ultra fast netlist readers	Netlist to schematics on the fly (within seconds)
32/64-bit database	Higher performance and increased capacity, for very large designs
Integrated waveform viewer	For easy signal tracing and simulation results analysis (accelerated VCD viewer)
Automatic clock tree and clock domain extraction and visualization	Faster detection and resolution for clock domain problems
Cone Window	Incremental schematic navigation for big designs
Verilog Netlist Export	Circuit fragments can be saved as Verilog netlist files
Tcl UserWare API	Allows interfacing with tool flow and definition of electrical rule checks
Netlist to schematics	Verilog viewer, EDIF viewer, and LEF/DEF viewer in one tool allows debugging of almost any netlist file format (incl. Liberty library support)
Powerful GUI	Multiple views, including tree, schematic, waveform, cone and source file for increased circuit understanding plus drag-and-drop between different views

Company Contact
Concept Engineering GmbH · Bötzinger Str. 29 · 79111 Freiburg · Germany
Tel: +49-761- 47094-0 · Fax: +49-761- 47094-29 · Email: info@concept.de · http://www.concept.de