FIRSTEDA
ENABLING DESIGN
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ALINT-PRO™ | Design Rule Checking

Static Design Verification

ALINT-PRO™ is a static design verification solution that uncovers critical design issues early in the design cycle. Static analysis requires just RTL and SDC sources and does not involve simulation, therefore no additional input (e.g. stimulus or assertions) is required to run analysis. This makes it rather easy to begin using ALINT-PRO quickly and begin focusing on design issues rather than the creation of complex verification artifacts.

ALINT-PRO covers a wide range of design issues including RTL and post-synthesis simulation mismatches, clock and reset trees analysis, clock domain crossings, proper design partitioning, DFT verification, design coding for reuse and portability, and many more.

Key Benefits/Top Features

Static Design Verification – performs analysis based on RTL and SDC sources and does not require complicated setup

DO-254 Support – includes dedicated ruleset for safety critical designs to achieve compliance with DO-254 guidelines

Schematic Visualization – efficient issues analysis, violated paths representation in graphical form and clock domains highlight

CDC Verification – obtain all RTL and CDC checks in the same product with ALDEC_CDC rule plug-in and achieve best possible linting results

DFT Verification – check for clock and reset controllability from external ports in the RTL design stage

Design Constraints – easy design setup (reuse of existing constraint files), facilitate initial design constraints file creation

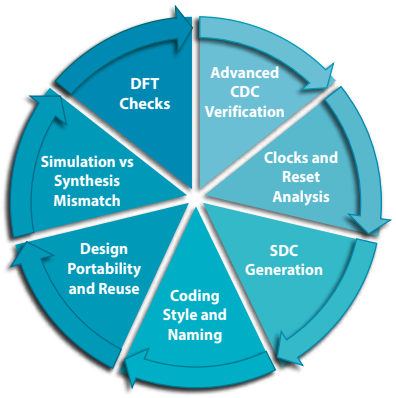
Design Constraints Extension – increase analysis quality by proper verification of IP's, behavioral modules and black boxes

Industry Proven Guidelines

The linting process is not simply detecting design faults but also involves the reuse of third party design expertise and leveraging quality code.

ALINT-PRO supports rule checks based on STARC (Semiconductor Technology Academic Research Center) and RMM (Reuse Methodology Manual) guidelines to utilize best practices in design development used by major semiconductor companies.

For safety critical designs, ALDEC offers DO-254 rule plug-in focused on design stability and is recommended to help achieve design compliance with the DO-254 standard.



ALDEC Basic and ALDEC Premium rule plug-ins capture the combined knowledge of Aldec customers and in-house design experts and can supplement the above plug-ins.

ALINT-PRO contains a powerful Policy Editor to quickly build an efficient rules configuration based on design needs.

CDC Verification

ALINT-PRO features an optional ALDEC_CDC rule plug-in, which enables the full power of Clock Domain Crossing (CDC) and RTL analysis in a single product. It enhances verification with dynamic checks based on assertions and metastability emulation and offers additional debug capabilities such as highlighting of clock domains in the Schematic Viewer, and navigating over the detected clock domain crossings and identified synchronizers.

DFT Verification

ALINT-PRO supports a dedicated set of rules to verify clock and reset controllability from external ports in the RTL design stage to make design testing easier on subsequent design stages.

STANDARDS

IEEE

STARC

PARTNERS

achronix SEMICONDUCTOR CORPORATION

intel

LATTICE

Microsemi

XILINX

FEATURES	PRODUCT CONFIGURATIONS
Supported Standards	ALINT-PRO
Verilog® IEEE 1364 (1995, and 2001)	•
SystemVerilog® IEEE 1800 (2005 and 2009)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Rule Libraries	
ALDEC BASIC (VHDL and Verilog)	•
ALDEC PREMIUM (VHDL and Verilog)	ALDEC PREMIUM Option
STARC (VHDL and Verilog)	STARC VHDL/VLOG Option
DO254 (VHDL and Verilog)	DO254 VHDL/VLOG
ALDEC CDC (VHDL, Verilog and SystemVerilog)	ALDEC CDC Option
Core Mechanisms	
Clocks and Resets Auto-detection	•
Clock Domains Extraction	•
Metastability Insertion	ALDEC CDC Option
Assertion Generation	ALDEC CDC Option
Coverage Statements for Crossings	ALDEC CDC Option
SDC Generation	•
Vendor Library Components Support	•
Combinational Feedbacks Detection	•
Custom Synchronizers Description	•
DFT Checks	STARC VHDL/VLOG Option
Debug Capabilities	
Schematic Viewer and Control Schematics	Schematics Option
Clocks and Reset Viewer	•
Hierarchy Viewer	•
Violation Viewer	•
CDC Viewer	ALDEC CDC Option
CDC Schematics	ALDEC CDC + Schematics Option
Design Management	
Project Manager	•
File Browser	•
Flow Manager	•
Library Manager	•
Policy Editor	•
Waiver Editor	•
Auto-Complete and Code Templates	•
Tasks Management	•
Active-HDL, Riviera-PRO, Vivado, and Quartus Projects	•
Supported Platforms	
Windows® 10/8.1/8/7/Vista/2003 32/64 bit	•
Linux 32/64 bit	•

Design Constraints Setup

ALINT-PRO can read SDC™ files for project configuration. This allows reusing existing configuration files for linting setup, making it easier for the designer to work with.

The tool can automatically generate initial SDC file, which can be a good starting point for design configuration. Such files contain clocks declarations (create_clock/create_generated_clock constraints), and set_input_delay/set_output_delay constraints generated for top-level design ports based on the combinational paths analysis.

Design Constraints Extension

ALINT-PRO offers a custom extension to design constraints, an easy to read and straightforward format to describe non-synthesizable behavioral modules, IP modules with protected code, vendor library cells, etc. Using constraints to describe module's interface substitutes black boxes in the netlist with equivalent models, which enable precise linting. It is also possible to describe custom synchronizer's interface with the help of constraints. Such synchronizers are checked to be instantiated on crossings between asynchronous domains and synchronized data is used in the destination domain.

Framework

ALINT-PRO provides a well-designed and tightly integrated GUI framework with intuitive interface and efficient issues analysis means. Framework includes:

Schematic Viewer – offers graphical representation of a full synthesized netlist and violated paths highlighting, and clock domains highlighting. Control Schematics graphically demonstrates the relations between clocks and resets. CDC Schematics is a specialized visualization for domain crossings and synchronizers;

Clocks and Resets Viewer – shows clock and reset networks with all pins and nets they are propagated through;

Violation Viewer – enables violations filtering by various criteria, cross-probing to HDL and Schematic, and gives access to summary data.

Active-HDL™, Riviera-PRO™, Vivado™ and Quartus™ projects can be automatically converted to ALINT-PRO format, significantly minimizing time required for design setup.

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